IN THE CLAIMS:

1. (Previously Presented) A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and an erase cycle time.

4. (Canceled)

5. (Canceled)

6. (Original) The method of claim 1, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

7. (Original) The method of claim 1, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

8. (Original) The method of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

9. (Previously Presented) A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of an erase cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

10. (Canceled)

11. (Previously Presented) The method of claim 9, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and a programming cycle time.

12. (Original) The method of claim 9, wherein said memory device is comprised of a gate insulation layer, a floating gate layer positioned above said gate insulation layer, an intermediate insulation layer positioned above said floating gate layer, and a control gate layer positioned above said intermediate insulation layer.

13. (Original) The method of claim 9, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

14. (Original) The method of claim 9, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

15. (Original) The method of claim 9, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

16.-20. (Canceled)

21. (Original) A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

22. (Original) A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.